WHAT IS CLAIMED IS:

1. A Phase-Locked Loop with multiphase clocks, said Phase-Locked Loop comprising:

a main loop comprising, coupled in series, a Phase Frequency Detector, a Main Charge Pump, a Main Loop Filter, a Multi-Phase Voltage Controlled Oscillator and a Phase-switching Fractional Divider;

a calibration loop coupled to the Phase Frequency Detector, the calibration loop comprising a Calibration Charge Pump, a Multiplexer and Y Calibration Loop Filters, with Y being an integer; and

Control Logic for controlling the Phase-Switching Fractional Divider and the Multiplexer,

wherein a Reference Frequency Signal is coupled to the Phase Frequency Detector and a Calibration Signal is coupled to the calibration loop,

the main loop further comprises a Phase-adjusting Block coupled to a Demultiplexer, the Phase-adjusting Block being arranged so as to receive at least one correction signal from the calibration loop.

2. The Phase-Locked Loop according to claim 1, wherein the Phase-adjusting Block comprises Y Low-frequency Delay Cells controlled by the Y Calibration Loop Filters.

3. The Phase-Locked Loop according to claim 2, wherein the at least one correction signal is a delay, specific to a phase, and corresponds to the Low-frequency Delay Cell corresponding to the phase.

4. A fractional-N frequency synthesizer comprising the Phase-Locked Loop according to claim 1.

5. An integrated circuit comprising at least one Phase-Locked Loop according to claim 1.

6. A digital mobile radio communication apparatus including at least one Phase-Locked Loop with multiphase clocks, said Phase-Locked Loop comprising:

a main loop comprising, coupled in series, a Phase Frequency Detector, a Main Charge Pump, a Main Loop Filter, a Multi-Phase Voltage Controlled Oscillator and a Phase-switching Fractional Divider;

a calibration loop coupled to the Phase Frequency Detector, the calibration loop comprising a Calibration Charge Pump, a Multiplexer and Y Calibration Loop Filters, with Y being an integer; and

Control Logic for controlling the Phase-Switching Fractional Divider and the Multiplexer,

wherein a Reference Frequency Signal is coupled to the Phase Frequency Detector and a Calibration Signal is coupled to the calibration loop,

the main loop further comprises a Phase-adjusting Block coupled to a Demultiplexer, the Phase-adjusting Block being arranged so as to receive at least one correction signal from the calibration loop.

7. The digital mobile radio communication apparatus according to claim 6, wherein the Phase-adjusting Block of said Phase-Locked Loop comprises Y Low-frequency Delay Cells controlled by the Y Calibration Loop Filters.

8. The digital mobile radio communication apparatus according to claim 7, wherein the at least one correction signal is a delay, specific to a phase, and corresponds to the Low-frequency Delay Cell corresponding to the phase.

9. The digital mobile radio communication apparatus according to claim 6, further including at least one fractional-N frequency synthesizer that comprises said Phase-Locked Loop.

10. The digital mobile radio communication apparatus according to claim 6, further including at least one integrated circuit that comprises said Phase-Locked Loop.

11. A method for synthesizing frequencies with a Phase-Locked Loop with multiphase clocks, said method comprising the steps of:

providing at least one Phase-Locked Loop that includes:

a main loop comprising, coupled in series, a Phase Frequency Detector, a Main Charge Pump, a Main Loop Filter, a Multi-Phase Voltage Controlled Oscillator and a Phase-switching Fractional Divider;

a calibration loop coupled to the Phase Frequency Detector, the calibration loop comprising a Calibration Charge Pump, a Multiplexer and Y Calibration Loop Filters, with Y being an integer; and

Control Logic for controlling the Phase-Switching Fractional Divider and the Multiplexer,

wherein the main loop further comprises a Phase-adjusting Block coupled to a Demultiplexer, the Phase-adjusting Block being arranged so as to receive at least one correction signal from the calibration loop;

applying a reference frequency signal to the Phase Frequency Detector of the Phase-Locked Loop; and

applying a Calibration Signal to the calibration loop of the Phase-Locked Loop.

12. The method according to claim 11, wherein the Phase-adjusting Block comprises Y Low-frequency Delay Cells controlled by the Y Calibration Loop Filters.

13. The method according to claim 12, wherein the at least one correction signal is a delay, specific to a phase, and corresponds to the Low-frequency Delay Cell corresponding to the phase.

14. The method according to claim 11, wherein a fractional-N frequency synthesizer comprises the Phase-Locked Loop.

15. The method according to claim 11, wherein an integrated circuit comprises the Phase-Locked Loop.

16. The method according to claim 11, wherein a digital mobile radio communication apparatus comprises the Phase-Locked Loop.